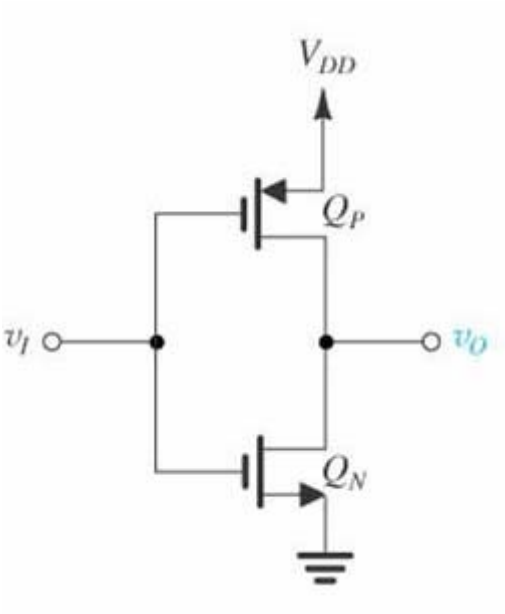
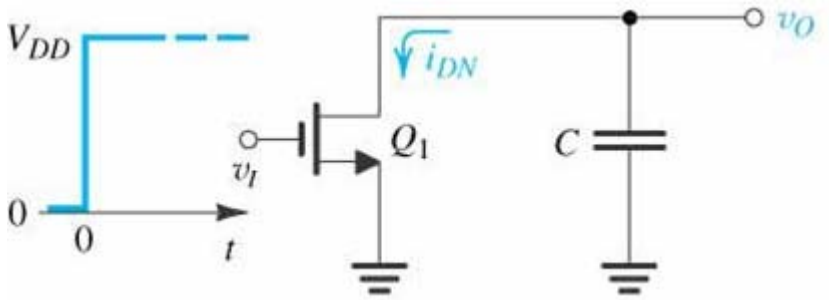
Lect. 21: CMOS Logic Gates (S&S 10.3)

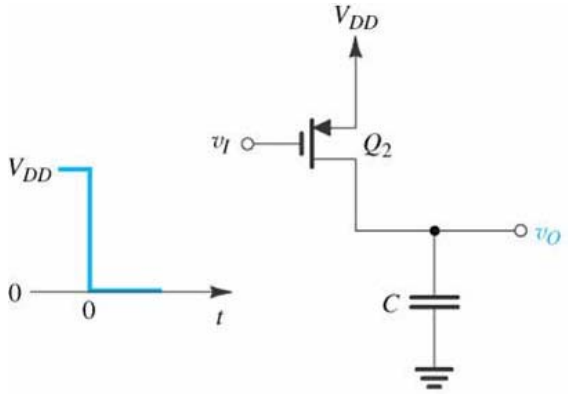
CMOS inverter



Pull Down



Pull Up

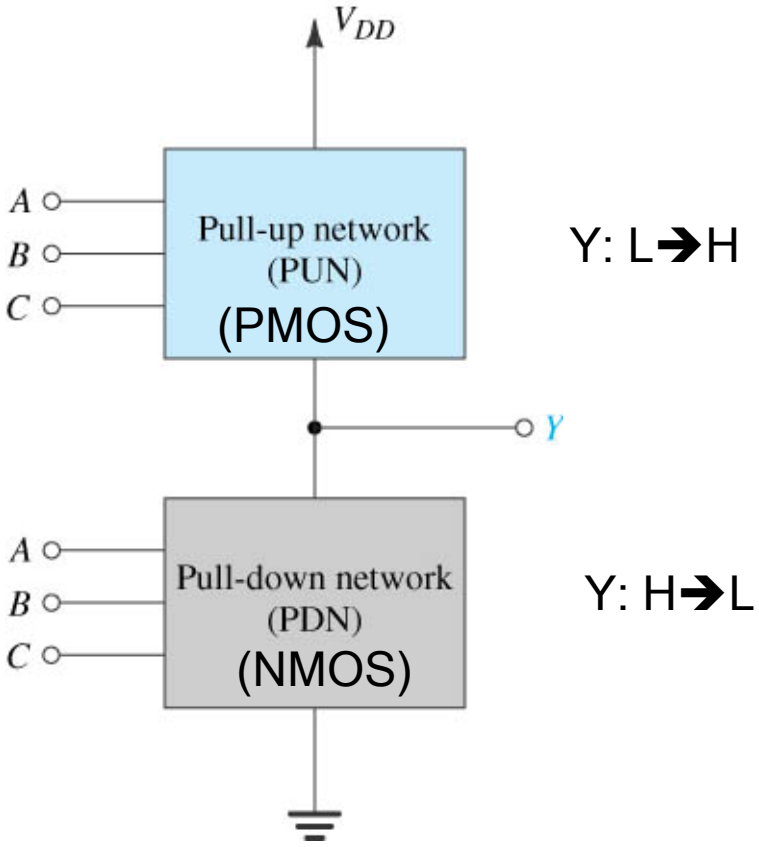


Different transistor acting for pull-down and pull-up operation

(NMOS) (PMOS)

Lect. 21: CMOS Logic Gates

CMOS Logic Gates

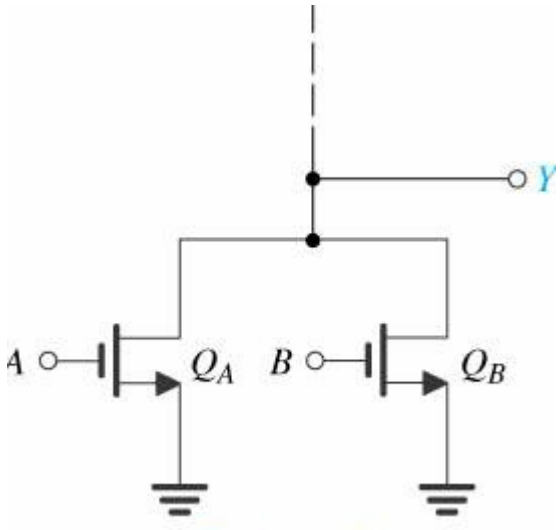


Y: L➔H

Y: H➔L

Lect. 21: CMOS Logic Gates

Examples of pull-down networks



Y pull-down, if A high OR B high

➔ Q_A or Q_B ON

For Y pull-up, A low AND B low

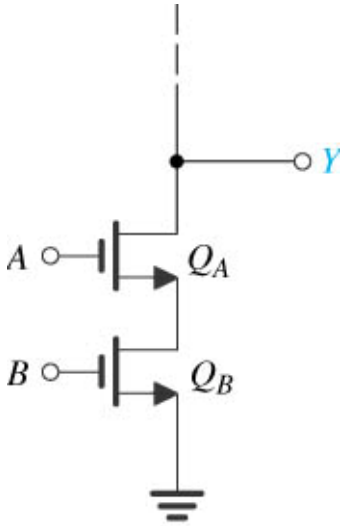
➔ Q_A and Q_B OFF

Logic Operation: $\bar{Y} = A + B$

➔ NOR Gate

Lect. 21: CMOS Logic Gates

Examples of pull-down networks



Y pull-down, if A high AND B high

➔ Q_A and Q_B ON

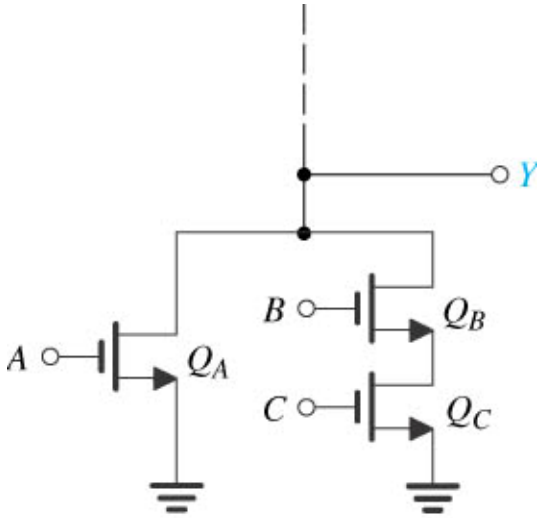
For Y pull-up, A low OR B low

➔ Q_A or Q_B OFF

Logic Operation: $\bar{Y} = AB$

➔ NAND Gate

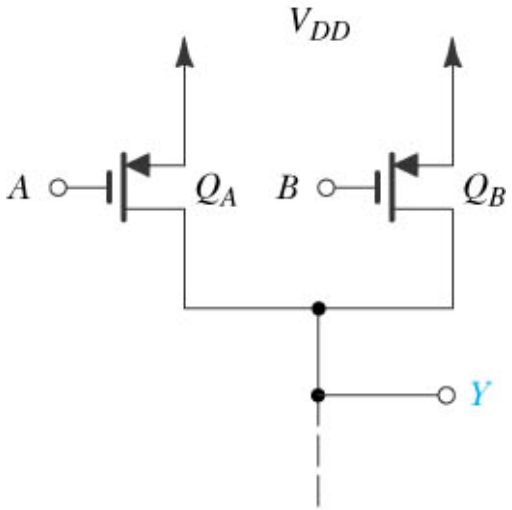
Examples of pull-down networks



$$\bar{Y} = A + BC$$

Lect. 21: CMOS Logic Gates

Examples of pull-up networks



Y pull-up, if A low OR B low

➔ Q_A or Q_B ON

For Y pull-down, A high AND B high

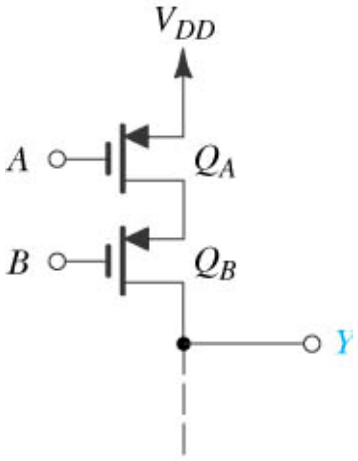
➔ Q_A and Q_B OFF

Logic Operation: $Y = \bar{A} + \bar{B}$

➔ NAND Gate

Lect. 21: CMOS Logic Gates

Examples of pull-up networks



Y pull-up, if A low AND B low

➔ Q_A and Q_B ON

For Y pull-down, A high or B high

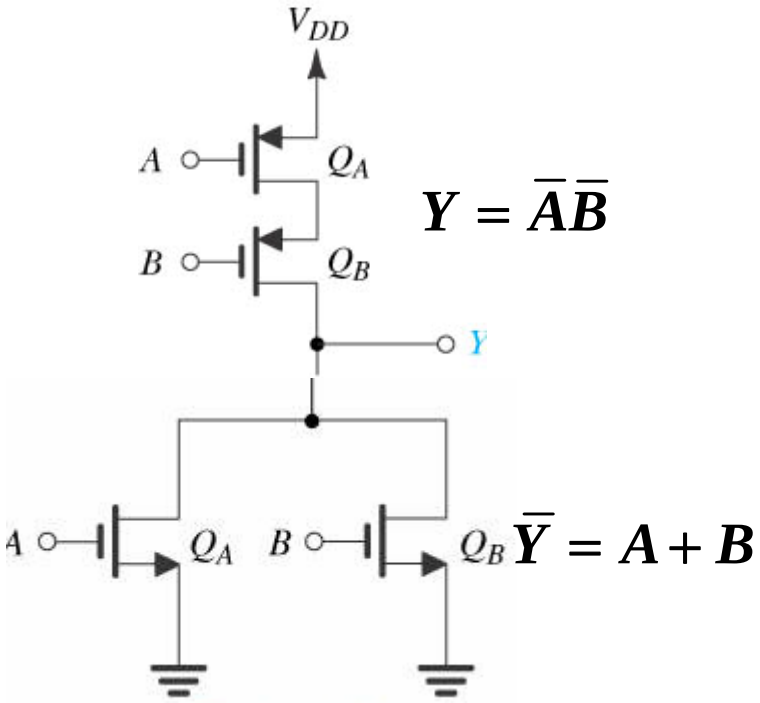
➔ Q_A or Q_B OFF

Logic Operation: $Y = \overline{A}\,\overline{B}$

➔ NOR Gate

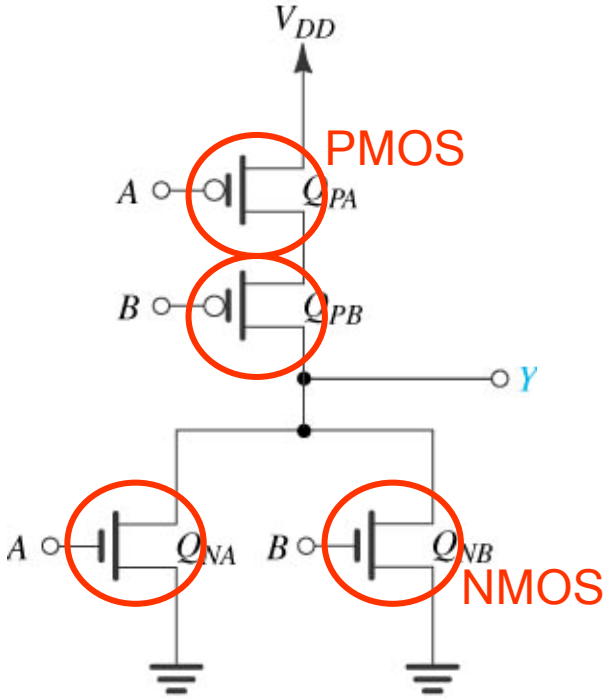
Lect. 21: CMOS Logic Gates

CMOS NOR Gate



$$Y = \overline{A}\,\overline{B}$$

$$\overline{Y} = A + B$$

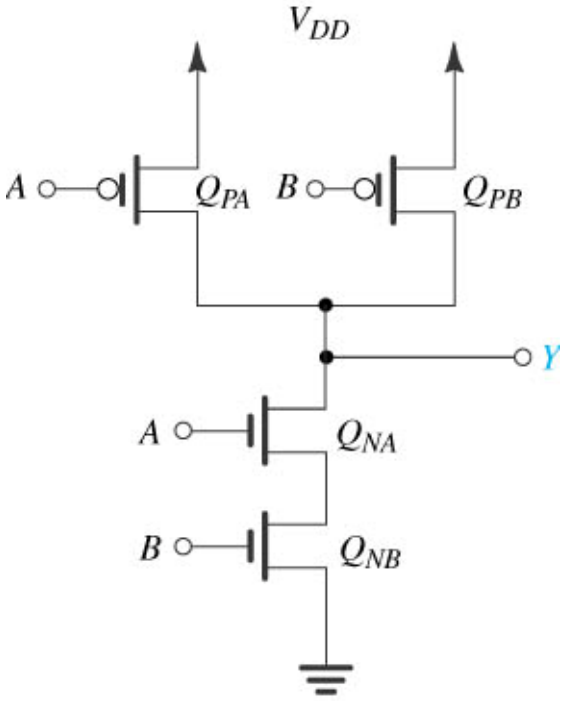


PUN: complemented input

PDN: complemented output

Structures of PUN and PDN have the duality property

Lect. 21: CMOS Logic Gates



CMOS NAND Gate

Lect. 21: CMOS Logic Gates

CMOS XOR (Exclusive OR)

A: 0 1 0 1
B: 0 0 1 1
XOR: 0 1 1 0

$Y = A\bar{B} + \bar{A}B$ ➔ PUN

$\bar{Y} = AB + \bar{A}\bar{B}$ ➔ PDN